Claims

1. Input circuit, in particular for a multiplexer, for phase controlling of a data input signal with a clock signal, comprising a flip-flop, wherein the data signal is fed to a clock input of the flip-flop and the clock signal is fed to the data input of the flip-flop, and wherein the data output of the flip-flop is used as a control signal of a locked loop.

2. Input circuit according to claim 1, comprising a further flip-flop, wherein the data signal is fed to a data input of the further flip-flop and the clock signal is fed to the clock input of the further flip-flop.

3. Input circuit according to claim 1, the data input signal being, in use, provided by output data of a data source, wherein the data source is arranged to control the phase of the output data in dependence of an adjusting signal which is input to the data source, wherein the locked loop delivers the adjusting signal to the data source.

4. Input circuit according to claim 2, wherein the locked loop is arranged to adjust the phase of the clock signal which is provided to the clock input of the further flip-flop.

5. Input circuit according to claim 4, wherein the locked loop is arranged to adjust the phase of the clock signal which is provided to the data input of the flip-flop.

6. Input circuit according to claim 4, wherein the locked loop comprises a controllable phase shifter (thus being a delay locked loop) and is arranged to adjust the phase of the clock signal which is provided to the data input of the flip-flop.

7. Multiplexer with an input circuit according to claim 1, the multiplexer having a plurality of data inputs to be provided with data signals, a data output and a clock input, wherein a said data signal is fed to a clock input of the flip-flop and the clock signal is fed to the clock input of the multiplexer.

8. Multiplexer with an input circuit according to claim 2, the multiplexer having a plurality of data inputs to be provided with data signals, a data output and a clock input, wherein a number of further flip-flops for a plurality of data signals is provided, which number corresponds to the number of data inputs of the multiplexer, and the clock input of the multiplexer is provided with a clock signal.

9. Method for phase controlling of a data signal with a clock signal comprising: scanning the clock signal with an edge of the data signal, deriving from the scanning result a control signal, using the control signal for adjusting the phase relationship between the data signal and the clock signal.